

BLF578XR; BLF578XRS

Power LDMOS transistor

Rev. 4 — 12 July 2013

Product data sheet

1. Product profile

1.1 General description

A 1400 W extremely rugged LDMOS power transistor for broadcast and industrial applications in the HF to 500 MHz band. This product is an enhanced version of the BLF578 using NXP's XR process to provide maximum ruggedness capability in the most severe applications without compromising the RF performance.

Table 1. Application information

Test signal	f (MHz)	V _{DS} (V)	P _L (W)	G _p (dB)	η _D (%)
pulsed RF	225	50	1400	23.5	69

1.2 Features and benefits

- Typical pulsed performance at frequency of 225 MHz, a supply voltage of 50 V and an I_{Dq} of 40 mA, a t_p of 100 μs with δ of 20 %:
 - ◆ Output power = 1400 W
 - ◆ Power gain = 23.5 dB
 - ◆ Efficiency = 69 %
- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (HF to 500 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

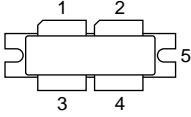
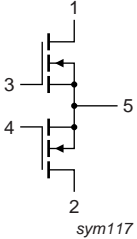
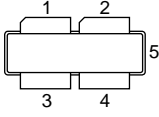
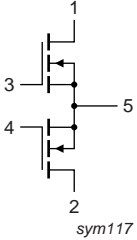
1.3 Applications

- Industrial, scientific and medical applications
- Broadcast transmitter applications



2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF578XR (SOT539A)			
1	drain1		 sym117
2	drain2		
3	gate1		
4	gate2		
5	source		
BLF578XRS (SOT539B)			
1	drain1		 sym117
2	drain2		
3	gate1		
4	gate2		
5	source		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BLF578XR	-	flanged balanced LDMOST ceramic package; 2 mounting holes; 4 leads	SOT539A
BLF578XRS	-	earless flanged balanced LDMOST ceramic package; 4 leads	SOT539B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

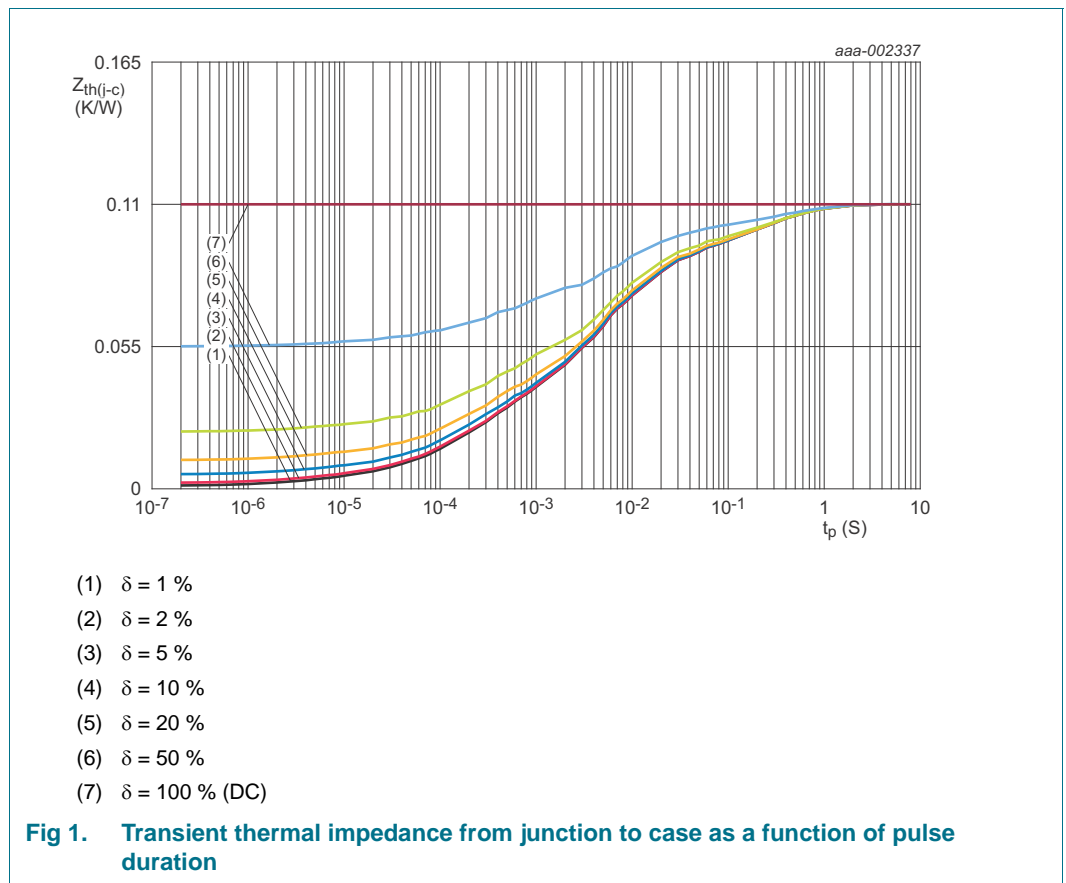
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	110	V
V_{GS}	gate-source voltage		-6	+11	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_j = 150\text{ }^\circ\text{C}$	[1][2] 0.11	K/W
$Z_{th(j-c)}$	transient thermal impedance from junction to case	$T_j = 150\text{ }^\circ\text{C}; t_p = 100\text{ }\mu\text{s}; \delta = 20\text{ }\%$	[3] 0.033	K/W

- [1] T_j is the junction temperature.
- [2] $R_{th(j-c)}$ is measured under RF conditions.
- [3] See [Figure 1](#).



6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ }^\circ\text{C}$; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 5.5\text{ mA}$	110	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 550\text{ mA}$	1.25	1.7	2.25	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 50\text{ V}$; $I_D = 20\text{ mA}$	0.8	1.3	1.8	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$	-	-	2.8	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $V_{DS} = 10\text{ V}$	-	77	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	280	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $I_D = 19.25\text{ A}$	-	0.07	-	Ω

Table 7. AC characteristics

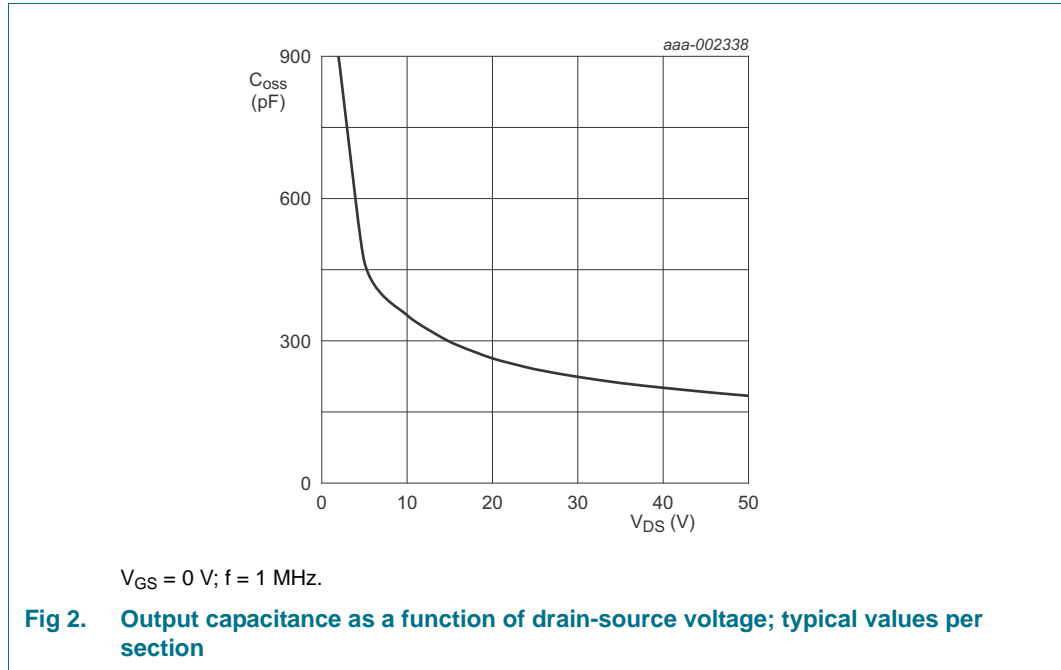
$T_j = 25\text{ }^\circ\text{C}$; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{rs}	feedback capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $f = 1\text{ MHz}$	-	5.5	-	pF
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $f = 1\text{ MHz}$	-	414	-	pF
C_{oss}	output capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $f = 1\text{ MHz}$	-	184	-	pF

Table 8. RF characteristics

Test signal: pulsed RF; $t_p = 100\text{ }\mu\text{s}$; $\delta = 20\%$; $f = 225\text{ MHz}$; RF performance at $V_{DS} = 50\text{ V}$; $I_{Dq} = 40\text{ mA}$; $T_{case} = 25\text{ }^\circ\text{C}$; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_L = 1400\text{ W}$	22	23.5	-	dB
RL_{in}	input return loss	$P_L = 1400\text{ W}$	-	-17	-13	dB
η_D	drain efficiency	$P_L = 1400\text{ W}$	65	69	-	%



7. Test information

7.1 Ruggedness in class-AB operation

The BLF578XR and BLF578XRS are capable of withstanding a load mismatch corresponding to $V_{SWR} > 65 : 1$ through all phases under the following conditions: $V_{DS} = 50\text{ V}; I_{Dq} = 40\text{ mA}; P_L = 1400\text{ W}$ pulsed; $f = 225\text{ MHz}$.

7.2 Impedance information

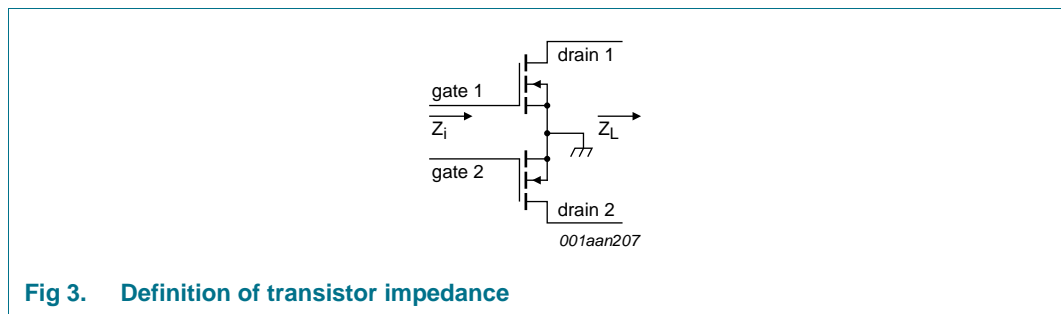


Table 9. Typical push-pull impedance

Simulated Z_i and Z_L device impedance; impedance info at $V_{DS} = 50\text{ V}$ and $P_L = 1400\text{ W}$.

f (MHz)	Z_i (Ω)	Z_L (Ω)
225	$2.36 - j2.78$	$2.45 + j0.86$

7.3 Test circuit

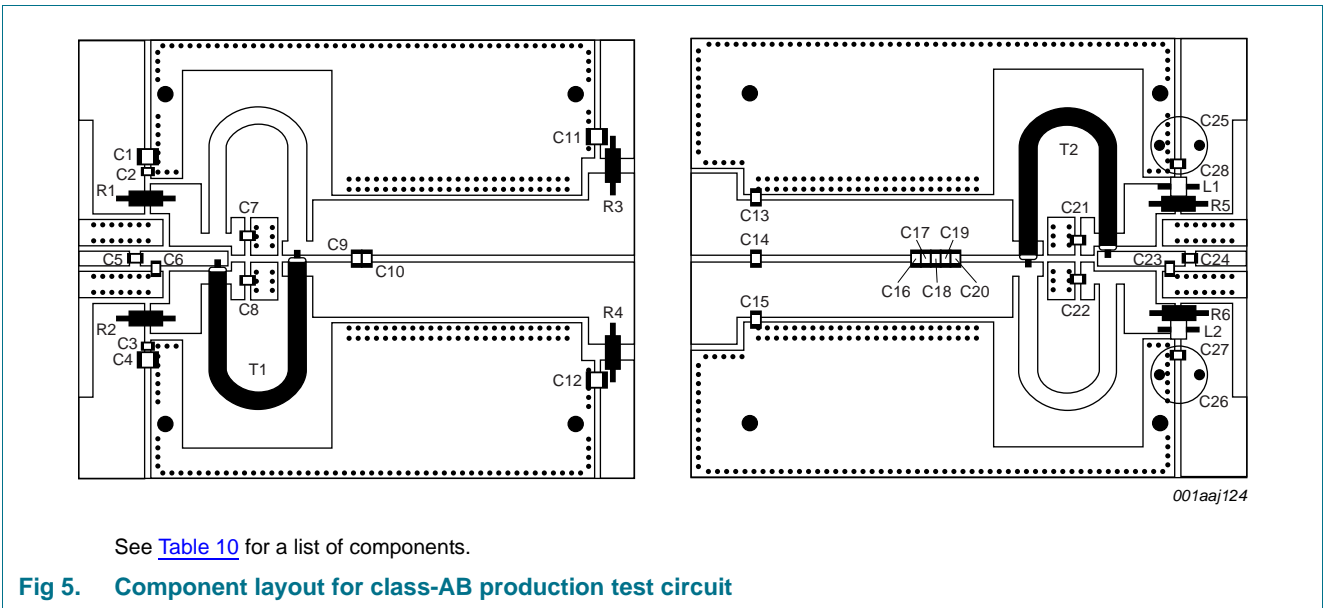
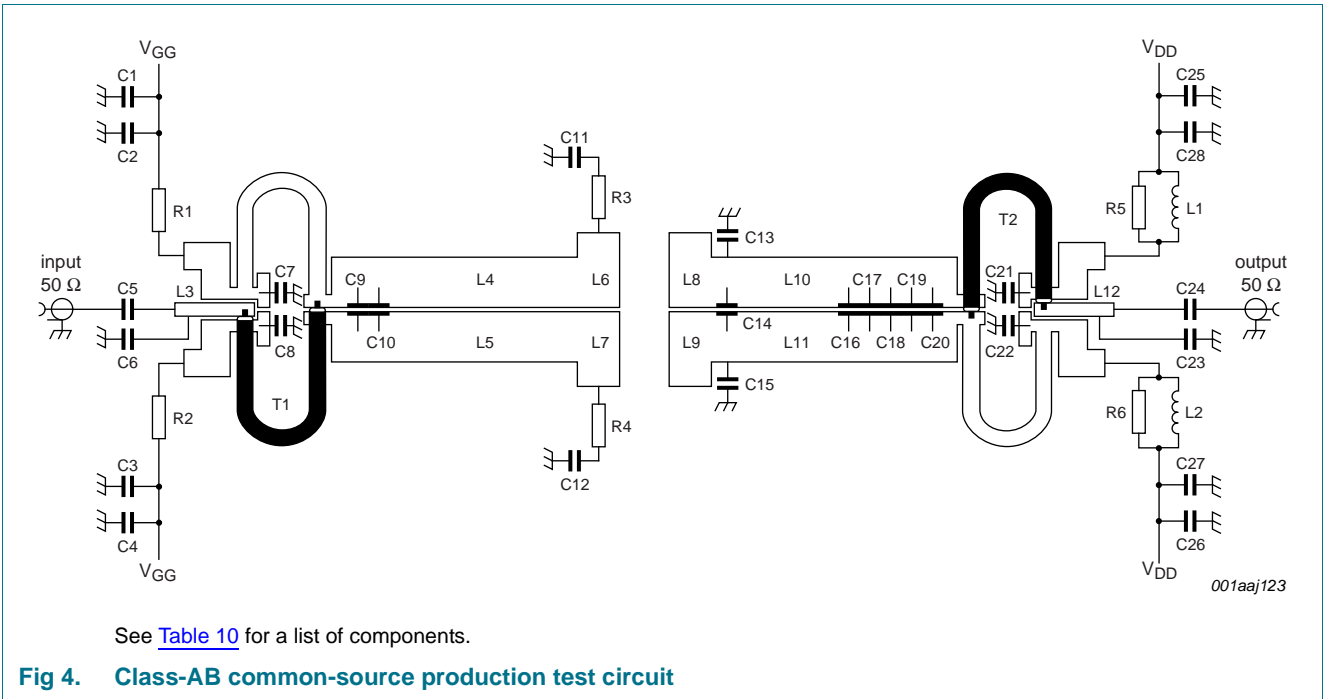


Table 10. List of components

For production test circuit, see [Figure 4](#) and [Figure 5](#).

Printed-Circuit Board (PCB): Rogers 5880; $\epsilon_r = 2.2$ F/m; height = 0.79 mm; Cu (top/bottom metallization); thickness copper plating = 35 μm .

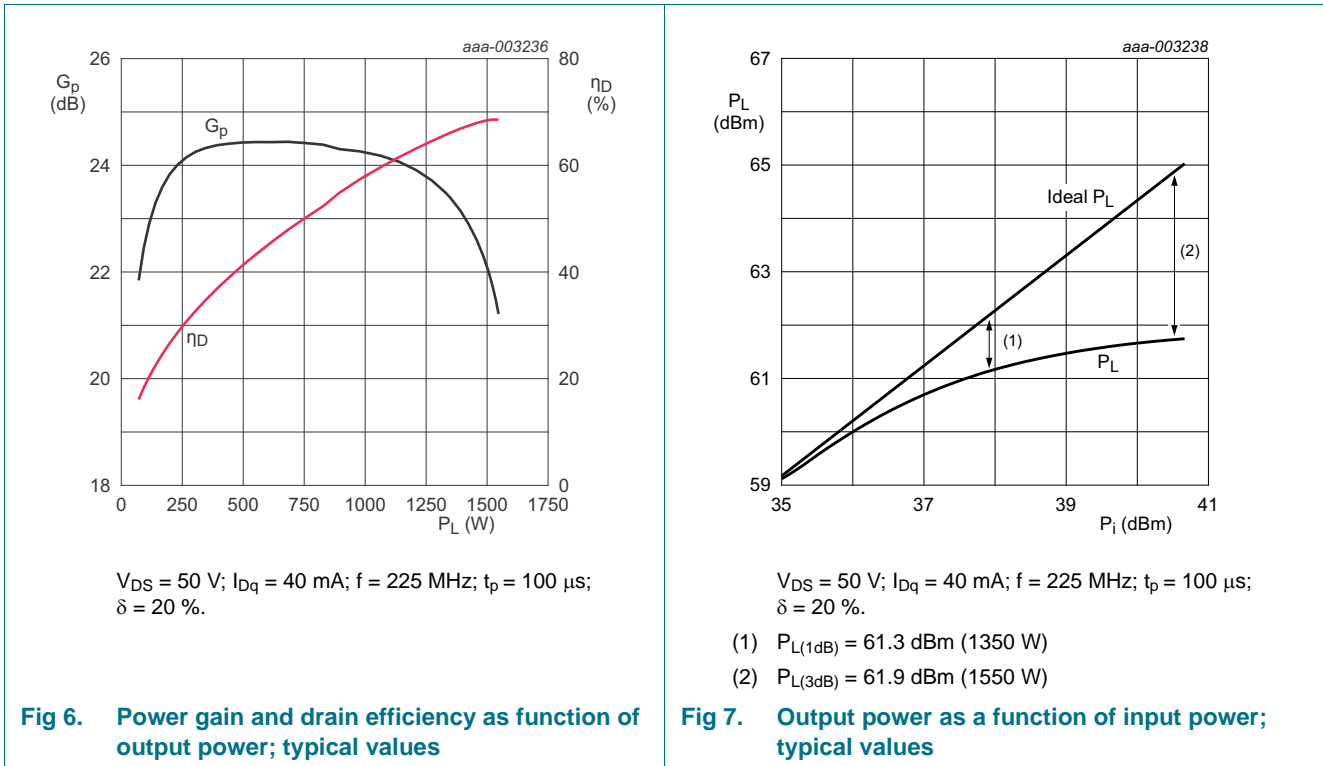
Component	Description	Value	Remarks
C1, C2, C11, C12	multilayer ceramic chip capacitor	4.7 μF	TDK4532X7R1E475Mt020U
C2, C3, C27, C28	multilayer ceramic chip capacitor	100 nF	Murata X7R 250 V
C5, C7, C8, C21, C22	multilayer ceramic chip capacitor	1 nF	[1]
C6	multilayer ceramic chip capacitor	30 pF	[1]
C9, C13, C15	multilayer ceramic chip capacitor	62 pF	[1]
C10	multilayer ceramic chip capacitor	51 pF	[1]
C14	multilayer ceramic chip capacitor	36 pF	[1]
C16, C17	multilayer ceramic chip capacitor	24 pF	[1]
C18	multilayer ceramic chip capacitor	30 pF	[1]
C19	multilayer ceramic chip capacitor	27 pF	[1]
C20	multilayer ceramic chip capacitor	9.1 pF	[1]
C23	multilayer ceramic chip capacitor	13 pF	[1]
C24	multilayer ceramic chip capacitor	16 pF	[1]
C25, C26	electrolytic capacitor	220 μF ; 63 V	
L1, L2	3 turns 1 mm copper wire	D = 2 mm; length = 3 mm	
L3, L12	stripline	-	(L \times W) 15 mm \times 2.4 mm
L4, L5, L10, L11	stripline	-	(L \times W) 47 mm \times 10 mm
L6, L7, L8, L9	stripline	-	(L \times W) 8 mm \times 15 mm
R1, R2	metal film resistor	2 Ω ; 0.6 W	
R3, R4	metal film resistor	20 Ω ; 0.6 W	
R5, R6	metal film resistor	1 Ω ; 0.6 W	
T1, T2	semi rigid coax	50 Ω ; 58 mm	EZ-141-AL-TP-M17

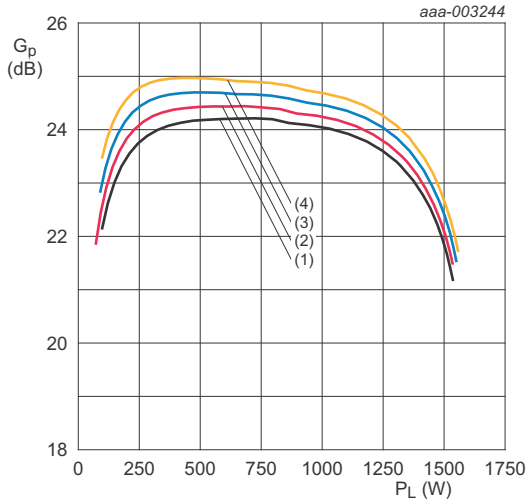
[1] American Technical Ceramics type 100B or capacitor of same quality.

7.4 Graphical data

The following figures are measured in a class-AB production test circuit.

7.4.1 1-Tone CW pulsed

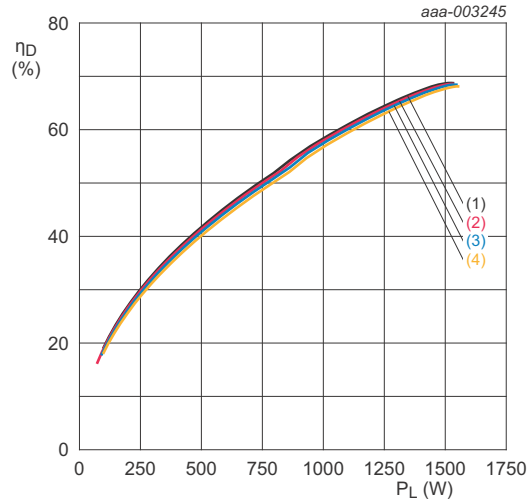




$V_{DS} = 50\text{ V}$; $f = 225\text{ MHz}$; $t_p = 100\text{ }\mu\text{s}$; $\delta = 20\text{ }\%$.

- (1) $I_{Dq} = 20\text{ mA}$
- (2) $I_{Dq} = 40\text{ mA}$
- (3) $I_{Dq} = 80\text{ mA}$
- (4) $I_{Dq} = 160\text{ mA}$

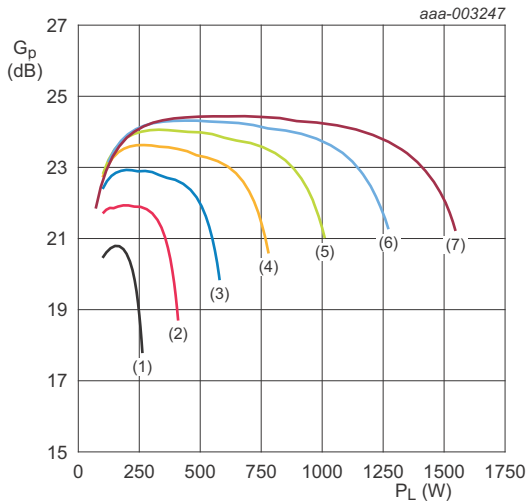
Fig 8. Power gain as a function of output power; typical values



$V_{DS} = 50\text{ V}$; $f = 225\text{ MHz}$; $t_p = 100\text{ }\mu\text{s}$; $\delta = 20\text{ }\%$.

- (1) $I_{Dq} = 20\text{ mA}$
- (2) $I_{Dq} = 40\text{ mA}$
- (3) $I_{Dq} = 80\text{ mA}$
- (4) $I_{Dq} = 160\text{ mA}$

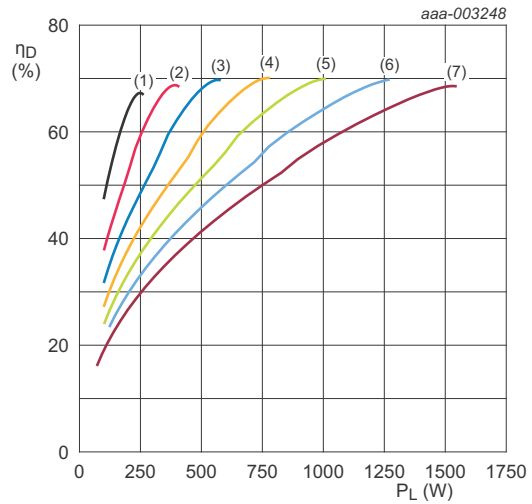
Fig 9. Drain efficiency as a function of output power; typical values



$I_{Dq} = 40\text{ mA}$; $f = 225\text{ MHz}$; $t_p = 100\text{ }\mu\text{s}$; $\delta = 20\text{ }\%$.

- (1) $V_{DS} = 20\text{ V}$
- (2) $V_{DS} = 25\text{ V}$
- (3) $V_{DS} = 30\text{ V}$
- (4) $V_{DS} = 35\text{ V}$
- (5) $V_{DS} = 40\text{ V}$
- (6) $V_{DS} = 45\text{ V}$
- (7) $V_{DS} = 50\text{ V}$

Fig 10. Power gain as a function of output power; typical values



$I_{Dq} = 40\text{ mA}$; $f = 225\text{ MHz}$; $t_p = 100\text{ }\mu\text{s}$; $\delta = 20\text{ }\%$.

- (1) $V_{DS} = 20\text{ V}$
- (2) $V_{DS} = 25\text{ V}$
- (3) $V_{DS} = 30\text{ V}$
- (4) $V_{DS} = 35\text{ V}$
- (5) $V_{DS} = 40\text{ V}$
- (6) $V_{DS} = 45\text{ V}$
- (7) $V_{DS} = 50\text{ V}$

Fig 11. Drain efficiency as a function of output power; typical values

8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads

SOT539A

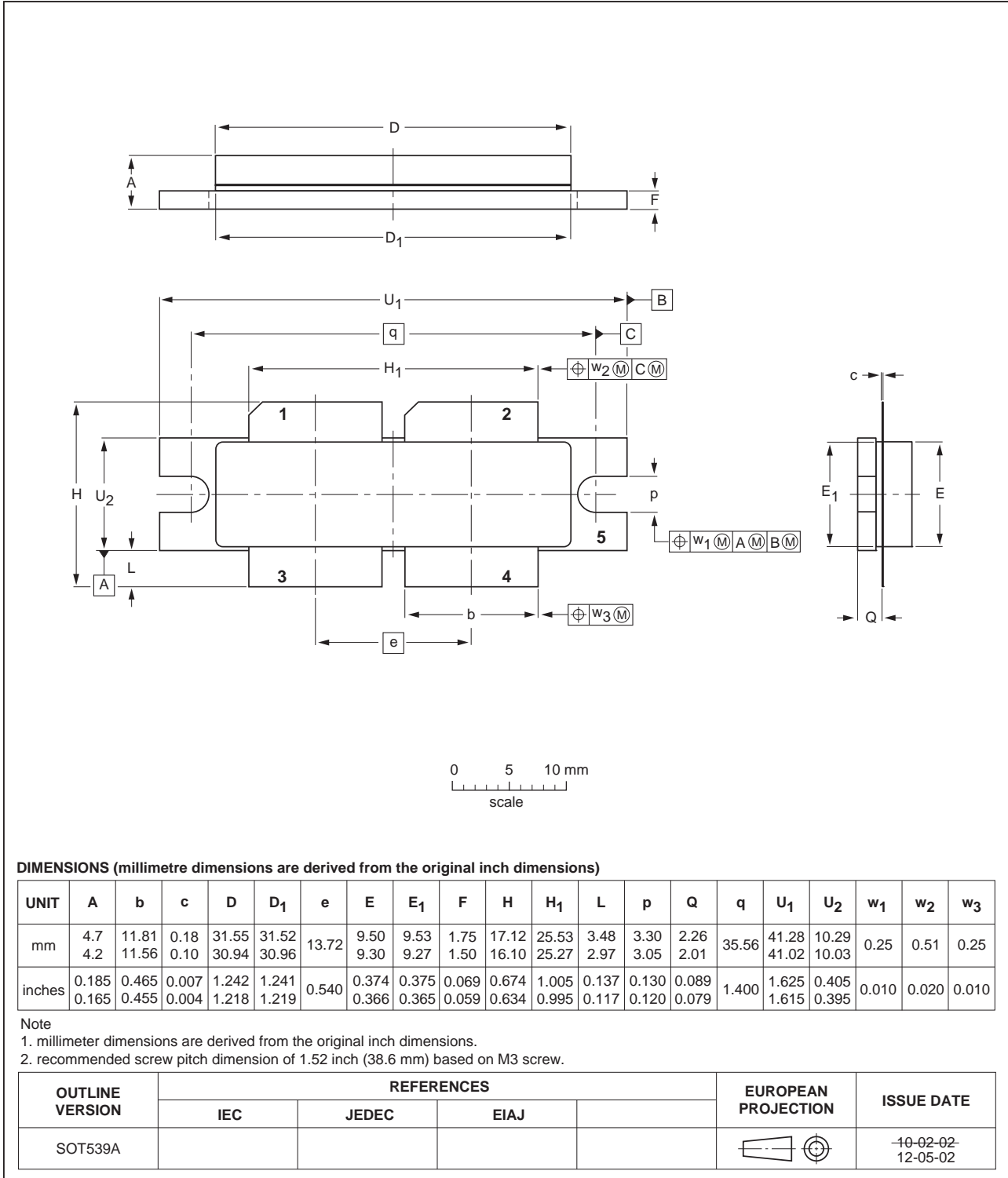


Fig 12. Package outline SOT539A

Earless flanged balanced ceramic package; 4 leads

SOT539B

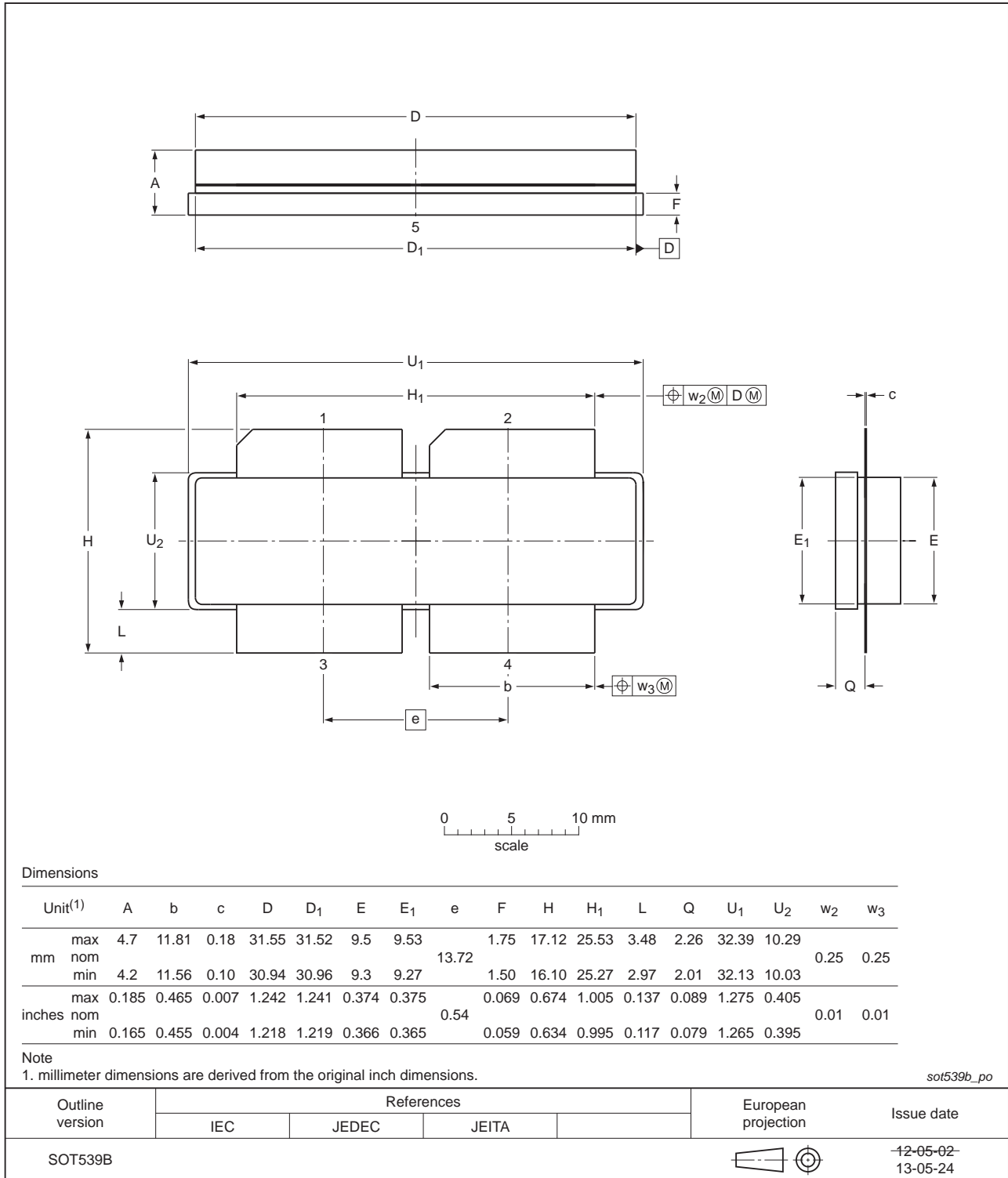


Fig 13. Package outline SOT539B

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
VSWR	Voltage Standing-Wave Ratio
XR	eXtremely Rugged

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF578XR_BLF578XRS v.4	20130712	Product data sheet	-	BLF578XR_BLF578XRS v.3
Modifications:	<ul style="list-style-type: none"> The package outline Figure 13 is updated. 			
BLF578XR_BLF578XRS v.3	20120625	Product data sheet	-	BLF578XR_BLF578XRS v.2
Modifications:	<ul style="list-style-type: none"> The status of this document has been changed to Product data sheet. 			
BLF578XR_BLF578XRS v.2	20120514	Preliminary data sheet	-	BLF578XR_BLF578XRS v.1
BLF578XR_BLF578XRS v.1	20120130	Objective data sheet	-	-

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12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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